WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a plurality of first data sense amplifiers, each first data sense amplifier being a voltage sense amplifier, each first data sense amplifier associated with data lines of a first type, the data lines of the first type leading from a bit line sense amplifier; and

a plurality of second data sense amplifiers, each second data sense amplifier including a current sense amplifier and a voltage sense amplifier, each second data sense amplifier associated with data lines of a second type, the data lines of the second type leading from a bit line sense amplifier.

2. The device of claim 1, wherein the data lines of the first type have lengths which are less than lengths of the data lines of the second type.

3. The device of claim 1, wherein the data lines of the first type have loads which are less than loads of the data lines of the second type.

4. The device of claim 1, further comprising:

a plurality of memory banks, a first set of the plurality of memory banks disposed closer to data pads of the semiconductor memory device than a second set of the plurality of memory banks, the first set of the plurality of memory banks associated with the data lines of the first type, and the second

set of the plurality of memory banks associated with the data lines of the second type.

5. The device of claim 4, wherein the data lines of the first type have lengths which are less than lengths of the data lines of the second type.

6. The device of claim 4, wherein the data lines of the first type have loads which are less than loads of the data lines of the second type.

7. The device of claim 4, wherein the data pads are located at a chip edge of the semiconductor memory device.

8. The device of claim 4, wherein the data pads are located substantially along a center of the chip of the semiconductor memory device.

9. The device of claim 4, further comprising:

a first multiplexer associated with each memory bank in the first set and the first multiplexer for selectively connecting the data line of the first type associated with the memory bank to one of the first data sense amplifiers;

a second multiplexer associated with each memory bank in the second set for selectively connecting the data line of the second type associated with the memory bank to one of the second data sense amplifiers; and

a third multiplexer associated with each of the first data sense

amplifiers for selectively connecting the first data sense amplifier to one of the data pads; and

a fourth multiplexer associated with each of the second data sense amplifiers for selectively connecting the second data sense amplifier to one of the data pads.

10. The device of claim 9, wherein the data lines of the first type have lengths which are less than lengths of the data lines of the second type.

11. The device of claim 9, wherein the data lines of the first type have loads which are less than loads of the data lines of the second type.

12. The device of claim 9, wherein the data pads are located at a chip edge of the semiconductor memory device.

13. The device of claim 9, wherein the data pads are located substantially along a center of the chip of the semiconductor memory device.

14. The device of claim 1, further comprising:

a plurality of memory banks, a first portion of each memory bank disposed closer to data pads of the multi-bank semiconductor memory device than a second portion of each memory bank, the first portions associated with the data lines of the first type, and the second portions associated with the

data lines of the second type.

15. The device of claim 14, wherein the data lines of the first type have lengths which are less than lengths of the data lines of the second type.

16. The device of claim 14, wherein the data lines of the first type have lengths which are less than lengths of the data of the second type such that output time from first and second data sense amplifiers is substantially the same.

17. The device of claim 14, wherein the data lines of the first type have loads which are less than loads of the data lines of the second type.

18. The device of claim 14, wherein the data pads are located substantially along a center of the chip of the semiconductor memory device.

19. The device of claim 14, further comprising:

a first multiplexer associated with each first portion for selectively connecting the data line of the first type associated with the first portion to one of the first data sense amplifiers;

a second multiplexer associated with each second portion for selectively connecting the data line of the second type associated with the second portion to one of the second data sense amplifiers; and

a third multiplexer associated with each of the first data sense amplifiers for selectively connecting the first data sense amplifier to one of the data pads; and

a fourth multiplexer associated with each of the second data sense amplifiers for selectively connecting the second data sense amplifier to one of the data pads.

20. The device of claim 19, wherein the data lines of the first type have lengths which are less than lengths of the data lines of the second type.

21. The device of claim 19, wherein the data lines of the first type have loads which are less than loads of the data lines of the second type.

22. The device of claim 19, wherein the data pads are located at a chip edge of the semiconductor memory device.

23. The device of claim 19, wherein the data pads are located substantially along a center of the chip of the semiconductor memory device.

24. The device of claim 14, further comprising:

first and second multiplexers associated with one of the first data sense amplifiers,

the first multiplexer associated with one of the first portions and the

first multiplexer for selectively connecting the data line of the first type associated with the first portion to the associated first data sense amplifier,

the second multiplexer associated with a different one of the first portions and the second multiplexer for selectively connecting the data line of the first type associated with the different first portion to the associated first data sense amplifier; and

third and fourth multiplexers associated with one of the second data sense amplifiers,

the third multiplexer associated with one of the second portions and the third multiplexer for selectively connecting the data line of the second type associated with the second portion to the associated second data sense amplifier,

the fourth multiplexer associated with a different one of the second portions and the fourth multiplexer for selectively connecting the data line of the second type associated with the different second portion to the associated second data sense amplifier.

25. The device of claim 24, wherein the data lines of the first type have lengths which are less than lengths of the data lines of the second type.

26. The device of claim 24, wherein the data lines of the first type have loads which are less than loads of the data lines of the second type.

27. The device of claim 24, wherein the data pads are located substantially along a center of the chip of the semiconductor memory device.

28. A semiconductor memory device, comprising:

a first plurality of data lines;

a second plurality of data lines, the second plurality of data lines having lengths which are greater than lengths of the first plurality of data lines;

a least one first data sense amplifier associated with the first plurality of data lines, each first data sense amplifier being a voltage sense amplifier; and

at least one second data sense amplifier associated with the second plurality of data lines, each second data sense amplifier including a current sense amplifier and a voltage sense amplifier.

29. The device of claim 28, wherein the data lines of the first type have loads which are less than loads of the data lines of the second type.